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DEVICE AND METHODOLOGY FOR REDUCING EFFECTIVE DIELECTRIC CONSTANT IN SEMICONDUCTOR DEVICES

Abstract

A method for manufacturing a structure includes providing a structure having an insulator layer with at least one interconnect and forming a sub lithographic template mask on the insulator layer. A selective etching step is used for etching the insulator layer through the sub lithographic template mask to form sub lithographic features near the at least one interconnect. A supra lithographic blocking mask may also be utilized. In another aspect, the method includes forming pinch off sections of sub lithographic size formed in a capping layer on the insulator layer. A semiconductor structure includes an insulator layer having at least one interconnect feature and at least one column formed in the insulator layer. A plurality of sub lithographic features formed on a top portion of the insulator layer and communicating with the at least one column is also provided. The plurality of sub lithographic features have a cross section or diameter less than any of the at least one column. A gap may be prohibited from forming on

or near scribe lanes and vias